

LZ2123Y

1/2 type Color CCD Area Sensor for PAL

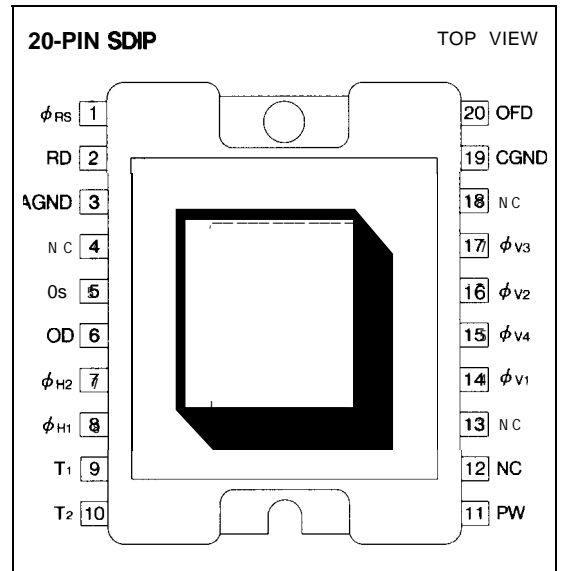
DESCRIPTION

LZ2123Y is a 1/2-type (8.0 mm) solid-state image sensor that consists of PN photo-diodes and CCDs (charge-coupled devices). Having approximately 320000 pixels (horizontal 542 X vertical 562), the sensor provides a high resolution stable color image.

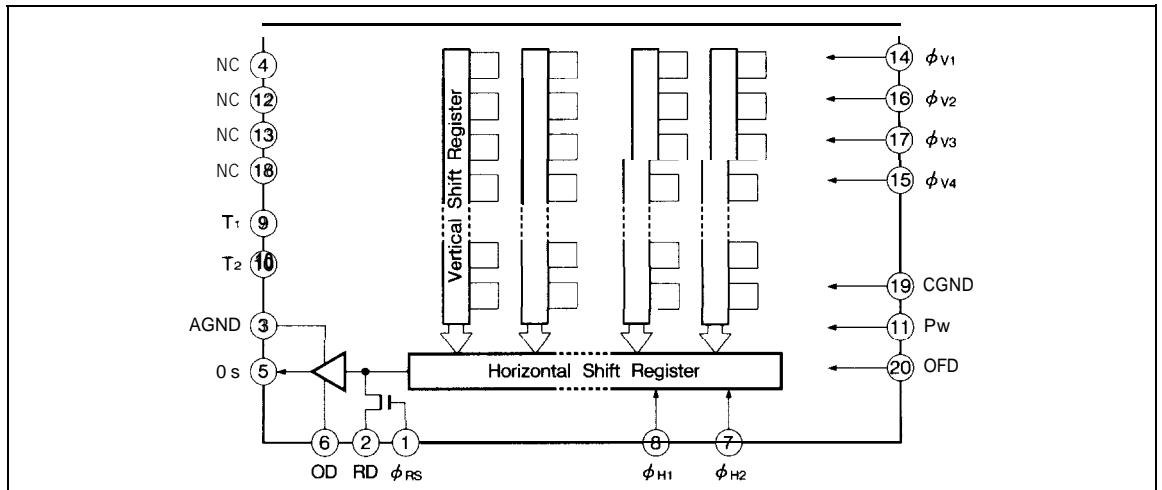
FEATURES

- Number of pixels : 512 (H) X 582 (V)
Pixel pitch : $12.8 \mu\text{m}$ (H) \times $8.4 \mu\text{m}$ (V)
Number of optical black pixels : Horizontal; front 2 and rear 28
- Complementary color filters of Mg, G, Cy and Ye
- Low fixed pattern noise and lag
- No sticking and no image distortion
- Blooming suppression structure
- Built-in output amplifier
- Variable electronic shutter (1/W to 1/1 0 000 s)
- Compatible with PAL standard
- Package : 20-pin SDIP[CERDIP](WDIP020-N-0600B)

FIN CONNECTIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
RD	Reset transistor drain
OD	Output transistor drain
Os	Video output
ϕ_{RS}	Reset transistor gate clock
$\phi_{V1}, \phi_{V2}, \phi_{V3}, \phi_{V4}$	Vertical shift register gate clock
ϕ_{H1}, ϕ_{H2}	Horizontal shift register gate clock
OFD	Overflow drain
PW	P type well
AGND	Analog part ground
CGND	Clock part around
T1, T2	Test terminal
NC	No connection

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

PARAMETER	SYMBOL	RATING	UNIT
Output transistor drain voltage	V_{OD}	0 to +18	v
Reset transistor drain voltage	V_{RD}	0 to +18	v
Overflow drain voltage	V_{OFD}	0 to +5.5	v
Test terminal, T1	V_{T1}	-0.3 to +18	v
Test terminal, T2	V_{T2}	0 to +18	v
Reset gate clock voltage	$V_{\phi RS}$	-0.3 to +18	v
Vertical shift register clock voltage	$V_{\phi V}$	-10 to +18	v
Horizontal shift register clock voltage	$V_{\phi H}$	-0.3 to +18	v
Voltage difference between PW and vertical clock	$V_{PW} - V_{\phi V}$	-26 to 0	v
Storage temperature	Tstg	-20 to +80	°C
Operating ambient temperature	Topr	-20 to +70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Operating ambient temperature		T_{OP}		25.0		°C	
Output transistor drain voltage		V_{OD}	14.5	15.0	16.0	V	
Reset transistor drain voltage		V_{RD}		V_{OD}		V	
Overflow drain voltage	When DC is applied	V_{OFD}	5.0	(adj.)	19.0	V	1
	When pulse is applied p-p level	$V_{\phi OFD}$	22.0			V	2
Analog part ground		AGND	—	0.0	—	V	
Clock part ground		CGND	—	0.0	—	V	
P-well voltage		V_{PW}	—9.5		$V_{\phi VL}$	V	
Test terminal, T1		V_{T1}	—	0.0	—	V	
Test terminal, T2		V_{T2}	—	V_{OD}	—	V	
Vertical shift register clock	LOW level	$V_{\phi V1L}, V_{\phi V2L}$ $V_{\phi V3L}, V_{\phi V4L}$	—9.5	—9.0	—8.5	V	
	INTERMEDIATE level	$V_{\phi V1I}, V_{\phi V2I}$ $V_{\phi V3I}, V_{\phi V4I}$		0.0		V	
	HIGH level	$V_{\phi V1H}, V_{\phi V3H}$	14.5	15.0	15.5	V	
Horizontal shift register clock	LOW level	$V_{\phi H1L}, V_{\phi H2L}$	—0.05	0.0	0.05	v	
	HIGH level	$V_{\phi H1H}, V_{\phi H2H}$	4.7	5.0	6.0	V	
Reset gate clock	LOW level	$V_{\phi RSL}$	—0.1	0.0	0.1	V	
	HIGH level	$V_{\phi RSH}$	8.0	9.0	10.0	v	
Vertical shift register clock frequency		$f_{\phi V1}, f_{\phi V2}$ $f_{\phi V3}, f_{\phi V4}$		15.63		kHz	
Horizontal shift register clock frequency		$f_{\phi H1}, f_{\phi H2}$		9.66		MHz	
Reset gate clock frequency		$f_{\phi RS}$		9.66		MHz	

NOTES :

1. When DC voltage is applied, shutter speed is 1/50 seconds.
2. When pulse is applied, shutter speed is less than 1/50 seconds

ELECTRICAL CHARACTERISTICS (Drive method : Field Accumulation)

($T_a = 25^\circ\text{C}$, Operating conditions : typical values for the recommended operating conditions, Color temperature of light source : 3200 K / IR cut-off filter (CM-500, 1 mmt))

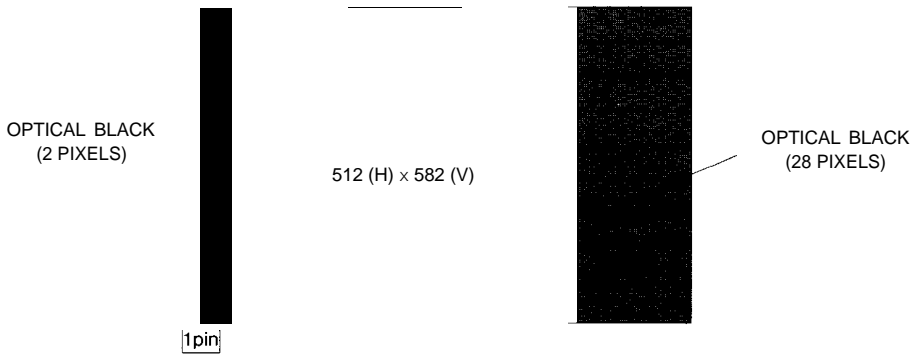
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Photo response non-uniformity	PRNU			10	%	2
Carrier saturation	Vsat	400			mV	3
Dark output voltage	Vdark		0.3	3.0	mV	1, 4
Dark signal non-uniformity	DSNU		0.6	2.0	mV	1, 5
Sensitivity	R	360	500		mV	6
Gamma	Y		1			
Smear ratio	SMR		0,005	0,016	%	7
Image lag	AI			1.0	%	8
Blooming suppression ratio	ABL	1000				9
Output transistor drain current	I _{oD}		4.0	8.0	mA	
Output impedance	R _o		300		Ω	
Dark noise	V _{noise}		0.2	0.3	mV	10
OB difference in level				1.0	mV	11
Vector breakup				7,0	, %	12
Line crawling				3.0	00	13
Luminance flicker				2.0	70	14

- The standard output voltage is defined as 150 mV by the average output voltage under uniform illumination.
- The standard exposure level is defined when the average output voltage is 150 mV under uniform illumination.
- V_{OFD} should be adjusted to the minimum voltage with that ABL satisfy the specification.

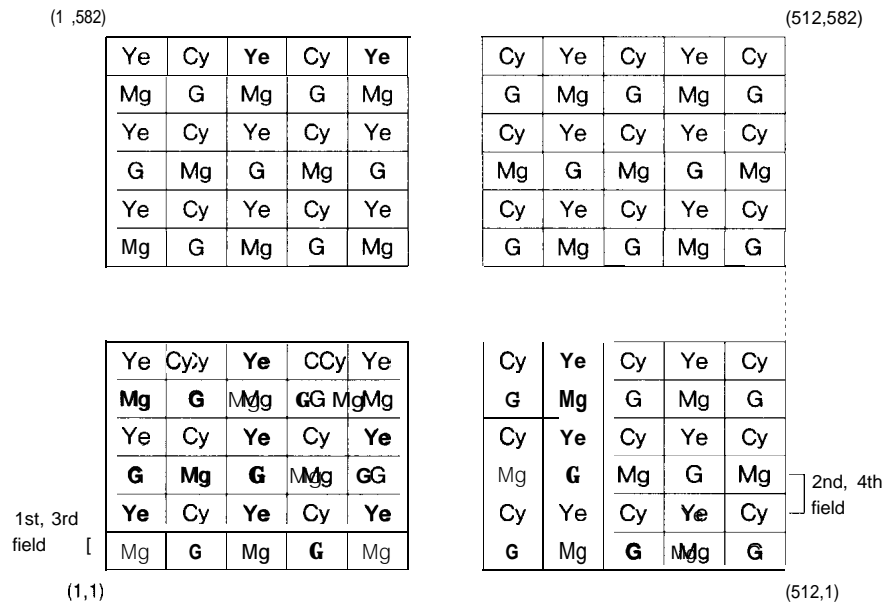
NOTES :

1. $T_a : +60^\circ\text{C}$
2. The image area is divided into 10x 10 segments. The segment's voltage is the average output voltage of all the pixels within the segment, PRNU is defined by $(V_{\text{max}} - V_{\text{min}})/V_o$, where V_{max} and V_{min} are the maximum and the minimum values of each segment's voltage respectively, when the average output voltage V_o is 150 mV.
3. The output voltage at the carrier peak when the carrier amplitude reaches maximum.
4. The average output voltage under a non-exposure condition.
5. The image area is divided into 10x 10 segments. OSNU is defined by $(V_{\text{dmax}} - V_{\text{dmin}})$ under the non-exposure condition where V_{dmax} and V_{dmin} are the maximum and the minimum values of each segment's voltage, respectively, that is the average output voltage over all pixels in the segment.
6. The average output voltage when a 1000lux light source attached with a 90°A reflector is imaged by a lens of F4, f50 mm.
7. The sensor is adjusted to position a V/I O square at the center of image area where V is the vertical length of the image area. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum of the pixel voltage in the V/I O square.
8. The sensor is exposed at the exposure level corresponding to the standard condition preceding non-exposure condition. AI is defined by the ratio between the output voltage measured at the 1st field during the non-exposure period and the standard output voltage.
9. The sensor is adjusted to position a V/I O square at the center of image area. ABL is the ratio between the exposure at the standard condition and the exposure at a point where a blooming is observed.
10. The RMS value of the dark noise (after CDS). The bandwidth range is from 100 kHz to 5.0 MHz. SC trap on.
11. The difference between the average output voltage of the effective area and the OB part under the non-exposure condition.
12. Observed with a vector scope when the color bar chart is imaged under the standard exposure condition,
13. The difference between the average output voltage of the (Mg + Ye), (G + Cy) line and the (Mg+Cy), (G+ Ye) line under the standard exposure condition.
14. The difference between the average output voltage of the odd field and the even field.

PIXEL STRUCTURE



COLOR FILTER ARRAY

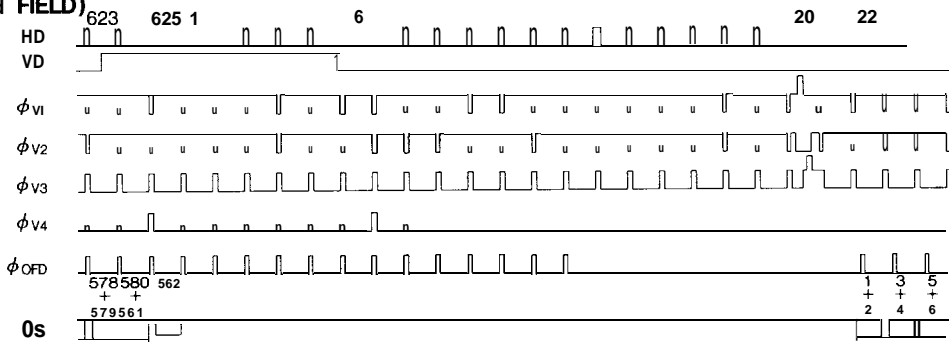


TIMING DIAGRAM EXAMPLE

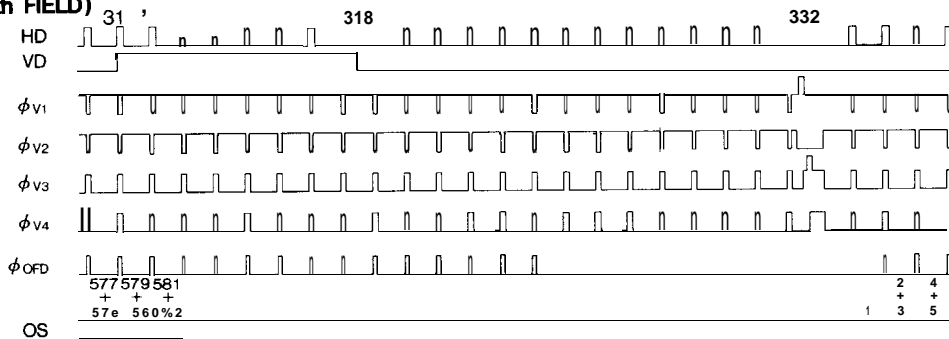
VERTICAL TRANSFER TIMING

Shutter speed
1 / 2000 s

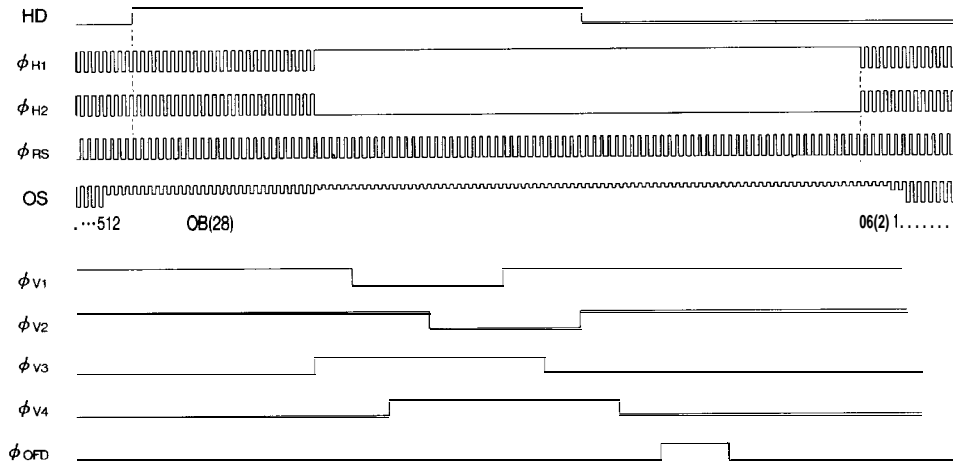
(1st, 3rd FIELD)



(2nd, 4th FIELD)



HORIZONTAL TRANSFER TIMING

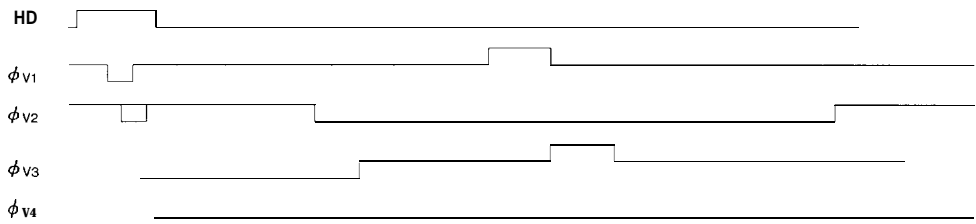


CCD AREA SENSORS

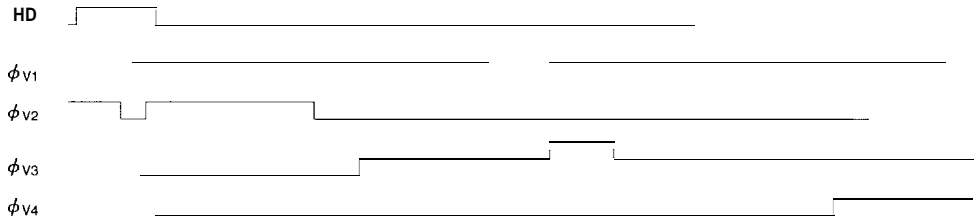
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READOUT TIMING

(1st, 3rd FIELD)



(2nd, 4rd FIELD)



SYSTEM CONFIGURATION EXAMPLE

